

REMARKS

The office action notes that "Grosbach does not specifically teach the controller reading from the same portion of a memory line in the same cycle on two different memory buses." One would think this is a substantial problem, but, according to the office action, it is one that can be overcome. In this regard, the office action points out that:

1. Grosbach provides the capability to map a portion of program memory space to the data memory space; and
2. This allows simultaneous program instruction and data access.

However, it is not seen how this has anything to do with reading out the same portion of a memory line. It is not seen how this has anything to do with reading the same portion of the memory line out on two different buses.


The office action argues that it would have been obvious to have arrived at the claimed feature because the result would have allowed program instructions processed to obtain speed advantages. This amounts to nothing more than the argument that, even though the reference does nothing like what is claimed since what is claimed is better, it would be obvious to do what is better. There is no rationale provided for why mapping program instructions and data memory spaces would lead to accessing or reading out the same portion of a memory line in the same cycle on two different buses, none of which is taught in the reference.

In fact, the reference says there is no need for two different buses and, most certainly, does not teach how to read out onto two different buses. See Summary at column 1, lines 59 and 60. The reference never contemplated reading the same portion of a memory line, but, clearly, is contemplating different memories being accessed at the same time, not the same portion of a memory line.

It is respectfully submitted that a *prima facie* rejection is not made out and the rejection should be reconsidered.

Respectfully submitted,

Date: February 4, 2009



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